A Successful Transition to Lead-free

Several factors drive electronics companies to switch to less-hazardous materials, including regulatory and market drivers. In 2003, the European Union (EU) published the RoHS Directive, banning the use of six substances above certain amounts. This article examines the lead-free implementation process one EMS provider performed.

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In January 2006, one EMS provider* conducted a lead-free implementation for an existing customer.** This implementation was conducted on an existing printed wiring board assembly (PWBA) used for medical equipment. Lead-free solder paste, a lead-free board surface finish, and lead-free component finishes were used. The board was previously manufactured using tin/lead solder paste.

Although this specific product is exempt from the RoHS Directive for lead-free electronics, there is tremendous value in conducting this transition in advance of possible end-user mandates or changes in RoHS product exemptions. By conducting this early transition, the issues and challenges of the assembly process can be identified and addressed cost efficiently.

Printed Wiring Board

The PCB has a footprint of about 7.5" × 9.2" with 16 layers and a thickness of 84 mils. A laminate material was chosen to meet the higher thermal requirements for lead-free assembly. The board is populated with 1,694 surface mount and thru-hole components on top and bottom sides. For components to be acceptable for lead-free assembly, they must have a lead-free component finish and the ability to withstand the higher-temperature profiles of lead-free processing. Of the 1,694 components, 1,675 were available with both qualifications. The remaining 19 components were missing at least one of these requirements. Upon completion of a review of component-supplier data, 13 BGAs were considered to be tin/lead. However, upon conducting X-ray fluorescence (XRF) scans during incoming quality inspection, a BGA that was claimed to be lead-free was discovered to contain tin/lead solder, increasing the number of tin/lead BGAs to 14.

Assembly Process

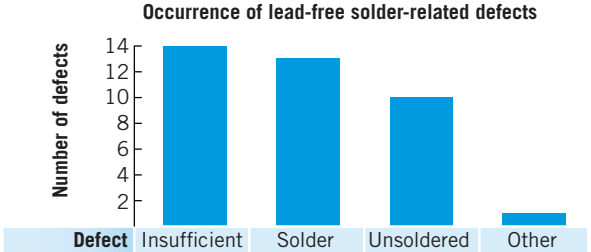
For the 19 components that did not meet both lead-free requirements, special processing was needed. The 14 tin/lead BGAs were micro-stenciled and sent to the reflow oven for the tin/lead profile. This included eight BGAs on the bottom side, and six BGAs on the top side. Four reflow passes were required to accommodate all SMT components. Five ICs were hand-soldered using a tin/lead solder paste.

The sequence of the major steps for the board assembly includes:

1. Tape-off 19 component locations on the stencil;
2. Bottom-side print and placement of SMT components;
3. Bottom-side reflow with lead-free profile (first pass);
4. Top-side print and placement of SMT components;
5. Top-side reflow with lead-free profile (second pass);
6. Micro-stencil bottom side and placement of eight BGAs;
7. Bottom-side reflow with tin/lead profile (third pass);
8. Micro-stencil top side and placement of six BGAs;
9. Top-side reflow with tin/lead profile (fourth pass);
10. Hand-solder five ICs;
11. Solder thru-hole components on rework machine.

The lead-free profile used for first and second passes was a ramp-to-peak profile with a peak temperature range of 240°–248°C, and a target time above liquidus (TAL) of 60–90 seconds. The tin/lead profile for third and fourth passes also had a ramp-to-peak profile with a target peak temperature range between 200° and 208°C. This was below 217°C to avoid unintentional reflow of the lead-free components that had been assembled during first and second reflow passes. Target TAL was 60–90 seconds.

For the tin/lead process, a water-soluble solder paste was used. Two different lead-free, water-soluble solder pastes were selected based on extensive lead-free printing experiments previously conducted.



Defect categories	Insufficient solder	Solder bridge	Unsoldered lead	Other
Count	14	13	10	1
Percent	36.8	34.2	26.3	2.6
Cumulative %	36.8	71.1	97.4	100

Figure 1. Occurrence of lead-free solder-related defects.

During the experiment, there was some lot-to-lot variation in the performance of one lead-free solder paste. Therefore, printing validation tests should be considered when using different solder paste lots. The stencil used in the assembly of tin/lead boards was stainless steel and laser-cut. It was 6-mils thick and uses a 10% standard reduction for tin/lead assembly.

A new stencil was fabricated to improve the printing process and the appearance of solder joints for lead-free electronics assembly. This stencil was also stainless-steel, laser-cut, and 6-mils thick. However, aperture sizes were changed to account for the different wetting properties of lead-free solder. For leaded devices and discrete components, aperture expansions were used in length, and a one-to-one, pad-to-aperture ratio was used for the width. For fine-pitch devices, aperture dimensions were based on pad size. Exact expansions and aperture dimensions used for the lead-free stencil are considered proprietary.

Thru-hole components were assembled using a rework machine. The lead-free solder used was the SAC 305 alloy, and the pot temperature was 285°C. The boards were preheated to 120°C, and the typical dwell time for soldering was 9–11 seconds.

Various test-and-inspection efforts were conducted for the 18 lead-free boards, including automated optical inspection (AOI), laminography, post-touch-up, X-ray inspection, post-inspection, continuity test, functional test, burn-in test, and final inspection. In total, 65 defects were identified and related to either manufacturing-process issues or soldering issues.

Design of Experiment — Lead-free Boards

A full factorial design was used to evaluate the influence of two factors on the quality of the lead-free boards: board surface finish and stencil design. Three levels were used for surface finish: organic solderability protectants (OSPs), immersion silver, and electroless nickel immersion gold (ENIG). Tin/lead and lead-free stencil designs were used. Therefore, there were six unique treatment combinations. Three replicates were used for each treatment combination, for a total of 18 runs. Table 1 illustrates the factorial design and number of total defects identified during the test-and-inspection process.

The null hypothesis used for this experiment is that the expected number of defects for different treatment combinations within the experimental design will be the same. The alternative hypothesis is that the expected number of defects for different treatment combinations within the experimental design will not be the same. Based on analysis of variance (ANOVA) results, there is no statistical difference between the quantity of defects found when comparing boards based on surface finish, stencil design, or any interactions of these two factors.

TABLE 1

Lead-free board test-and-inspection process

Board Number	Surface Finish	Stencil	Total Defects
1	OSP	Tin/lead	7
2	OSP	Tin/lead	2
3	OSP	Tin/lead	1
4	OSP	Lead-free	7
5	OSP	Lead-free	5
6	OSP	Lead-free	5
7	Imm. Ag	Tin/lead	1
8	Imm. Ag	Tin/lead	2
9	Imm. Ag	Tin/lead	3
10	Imm. Ag	Lead-free	1
11	Imm. Ag	Lead-free	4
12	Imm. Ag	Lead-free	5
13	ENIG	Tin/Lead	3
14	ENIG	Tin/lead	2
15	ENIG	Tin/lead	4
16	ENIG	Lead-free	6
17	ENIG	Lead-free	4
18	ENIG	Lead-free	3

Comparison of Tin/lead and Lead-free

To conduct a comparison of the results for tin/lead and lead-free processes, two previously completed tin/lead work orders were selected at random. These included 94 boards that were assembled in 2004. Table 2 lists data for tin/lead and lead-free defects identified. It can be stated with 95% confidence that there is no difference between the median defects per board or defect variances between tin/lead and lead-free processes.

Six Sigma Metrics

Three common process-performance metrics used are Defects per Unit (DPU), Defects per Million Opportunities (DPMO), and sigma level. DPU is total number of defects identified on all units, divided by the number of units. To calculate the number of opportunities for DPMO, it is necessary to determine the number of ways a defect can occur on each item. An opportunity for defect could occur for each lead of a component, as well as in placing the correct component in the correct manner. The total number of opportunities for defects for each board in this experiment was calculated at 16,134. Sigma level describes the capability of a process to meet a specification. A higher sigma level indicates that a process has a greater tendency to perform within its specification limits. Six sigma level is used to describe a process that has 3.4 DPMO.

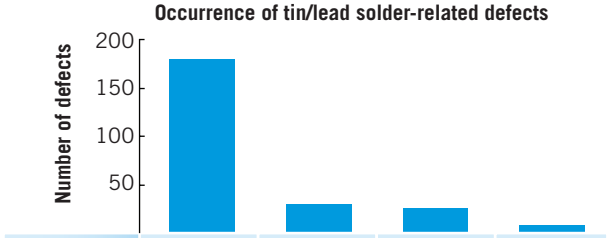
Tin/lead board assembly:
DPU = 4.03
DPMO = 249.9
Sigma level = ~5.0

Lead-free board assembly:
DPU = 3.61
DPMO = 223.8
Sigma level = ~5.0

Solder Paste-related Defects

The above analysis and metrics were based on total defects identified during the test-and-inspection process. This includes defects that are manufacturing-assembly related, as well as defects related to soldering. For this section, an analysis will be conducted for solder-related defects only.

In this report, defect categories considered to be related to manufacturing-assembly issues include: reversed components, missing components, bent pins, misplaced components, electrically-defective components, damaged components, and sheared components. Defect categories related to soldering issues include: solder bridges, unsoldered leads, tombstoned components, non-wetting, and insufficient solder. Based on ANOVA results, there is no statistical difference between the quantity of



Defect categories	Unsoldered lead	Tombstoned component	Solder bridge	Other
Count	179	29	25	8
Percent	74.3	12.0	10.4	3.3
Cumulative %	74.3	86.3	96.7	100

Figure 2. Occurrence of tin/lead solder-related defects.

TABLE 2

Tin/lead and Lead-free Defects (manufacturing- and solder-related)

Parameter	Tin/lead Process	Lead-free Process
Number of boards	94	18
Number of defects	379	65
Mean defects per board	4.03	3.61
Median defects per board	2.0	3.5
Standard deviation	4.56	1.94
Variance	20.83	3.78
Range	0–17	1–7

TABLE 3

Tin/lead and lead-free defects (solder-related only)

Parameter	Tin/lead Process	Lead-free Process
Number of boards	94	18
Number of defects	241	38
Mean defects per board	2.56	2.11
Median defects per board	1.0	2.0
Standard deviation	3.80	1.53
Variance	14.42	2.34
Range	0–4	0–14

defect found between boards based on board-surface finish, stencil design, or interactions of these two factors. Table 3 lists data for tin/lead and lead-free defects identified. It can be stated with 95% confidence that there is no difference between the median defects per board or defect variances between tin/lead and lead-free processes. Figure 1 shows type and quantity of solder-related defects identified during the test-and-inspection process for 18 lead-free boards. Figure 2 shows types and quantity of soldering-related defects for the 94 tin/lead boards.

Conclusion

The mean-defect level for the lead-free assembly process is not influenced by the three board-surface finishes or the two stencil designs used for this case study. Further, it can be stated with 95% confidence that there is no difference between the median defects per board or variance between the tin/lead and lead-free processes. These conclusions are consistent for the analysis of the total defects, as well as the analysis of solder-related defects only. SMT

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